Print ISSN: 0974-2115
www.jchps.com Journal of Chemical and Pharmaceutical Sciences

Design And Analysis Of Various Vlsi Optimization Techniques For Correlators

Sivasankari B[1*] and Poongodi P[2]

[1]Department of Electronics & Communication Engineering, SNS College of Technology, Coimbatore, Tamil Nadu
[2]Department of Electronics & Communication Engineering, Karpagam College of Engineering, Coimbatore, India

***Corresponding author: E-Mail: sanksnsct@gmail.com**

ABSTRACT

Background: This paper describes about correlator architectures with different VLSI optimization techniques such as parallel processing and pipelining. Both of these techniques are used to reduce the power consumption and to achieve high speed. Objective: To achieve high speed and low power consumption, VLSI optimization techniques such as parallel processing and pipelining technique is used. Results: Simulation is done using Xilinx ISE 13.2 tool with Verilog HDL (Verification Logarithmic Hardware Description Language) and it has been synthesized on Kintex7 (xc7k70t-fbg676) FPGAs for the multiplier less correlator and pre-compute correlator. When compared to parallel pre-compute correlator, parallel pre-compute correlator with pipelining reduces the delay by 20.77%. Conclusion: Up to certain limit pipelining provides significant performance gains with little increase in chip area. It also reduces glitching in the circuit. Throughput beyond that acheivable by pipelining can be attained by parallel architectures.

KEY WORDS: Optimization, Parallel Processing, Pipelining, Correlator.

1. INTRODUCTION

Now a days, wireless equipments are parts of everyone's life. In every fragile from mobiles to computer, Broadband Wireless Access (BWA), internet is most popularly used without the use of a wired modem connection. In wireless system, the data's are transmitted through radio waves. It is possible for extended range of communications, which is not possible with the use of wires. Some other wireless accesses are Wi-Fi and WiMAX. The operation of Wi-Fi and WiMAX is similar, but WiMAX operates at high speed and it is used for a large number of users. It is a multi-carrier modulation technique, where the closely spaced sub carrier signals are used to carry the data to the channels in a parallel manner. These subcarriers are orthogonal to each other. To eliminate the Inter Symbol Interference (ISI), the sub carriers should be non-overlapped. For a complete elimination of ISI there must be some guard interval between OFDM symbols. when the correlation scheme is used, the Hardware complexity of MIMO-OFDM synchronization is reduced based on time-multiplexing technique.

C.Visweswariah (1997) proposed the circuit optimization technique to maintain timing accuracy. G. Hazari et al proposed that the VLSI optimizing the flow,which suitable for compilers, design procedures and real-time allocations on-chip modules. In buffer insertion algorithm, Uttraphan proposed a new technique which optimize the interconnect power and delay consumption of buffers using dynamic programming. Fatemeh Kashfi (2011) presenting a variety of analytical methods to optimize power and delay of VLSI system.

An FPGA architecture could be exploited in for implementing the wireless communication protocols. The precomputation based correlators also presented in for improving throughput of the wireless system.

Correlator is a digital device that takes two Nyquist-sampled digital streams representing the voltages which is present in one or more radio receivers and computes the cross-correlation function as a time lag function. Correlation is a mathematical operation that is similar to convolution. Correlation uses two signals to generate third signal. Each correlation algorithms are based on the correlation of the received signal. Multiplier less correlator is designed to replace the use of DSP slices. It reduces area, delay and power consumption. Also it can be used in any FPGA architecture. Based on a cross - correlation algorithm the out- performance is improved. So it needs less hardware operators(components) than the classic correlator. In 2014, Anandh Leno et.al proposed design of Resource Efficient Low Power Correlator for Communication for optimization. The following optimization techniques are given for achieving higher throughput.

Parallel Processing: In DSP, parallel processing is a technique duplicating function unit to operate different tasks (signals) simultaneously. Accordingly, we can do the same signal processing for different signals based on the equivalent duplicated function units. Due to the features of parallel processing, the multiple outputs are generated by parallel DSP design, which results in higher throughput than not parallel. Reduced power consumption, not increase in clock speed, increased sample speed and Parallelism are the advantages of parallel processing.

Pipelining: One important technique used in most of the digital applications such as microcontrollers, DSP systems etc. is Pipelining. Its operation initiates from the basic idea of a water pipeline, where the water sent continuously without waiting for the water in the pipeline to bring out. On most DSP systems, the speed enhancement of the critical path is based on this pipelining operation. For example, either it can reduce the power consumption or increase

the clock frequency at the same speed of the DSP system. DSP48E1-based correlators can attain higher clock speeds only through a detailed pipelined design.

2. METHODS

Proposed Vlsi Optimization Based Correlators:

Parallel Pre-compute Correlator: The architecture of parallel pre compute correlator is shown in Fig.1. The proposed parallel correlator is mainly used in OFDM systems for timing synchronization. The size of the correlator and the number of registers is based on the input samples. The correlator coefficients are selected based on the preamble samples of the short OFDM signal. Preamble signal is used for transmitting time synchronization. The parallel correlator is also based on computation sharing technique. The product of the received sample with the complex correlator coefficients is estimated by the pre-compute and the selector unit. Pre-computed values are selected based on the multiplexer. Finally the addition process is done in parallel. Because of this parallel processing, it reduces the delay with some area overhead.

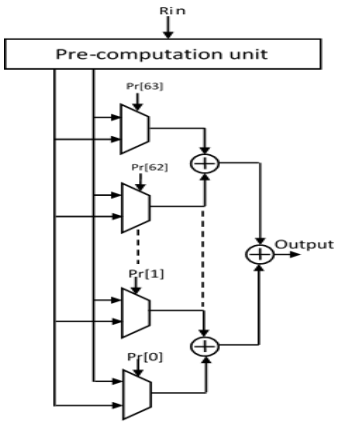

Figure.1. Architecture of Parallel Precompute Correlator

Parallel Precompute Correlator With Pipelining: The architecture of parallel pre-compute correlator with pipelining is shown in Fig.2. The correlator is implemented using parallel processing, pipelining and sharing technique. With the help of these techniques, the speed will be increased and the power consumption is reduced.

Here R is the 64 bit register and pr [0], pr[1]….pr[63] are preamble symbols. The basic components of this architecture are Multiplexer, Adder, pre-computation unit and registers. The pre-computed values are selected with the help of preamble symbols. The pre-computation unit computes the product of received sample with the complex correlator coefficients.

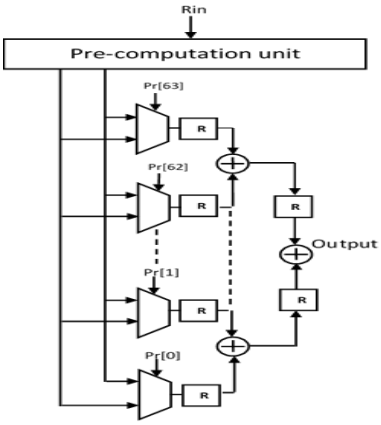

Figure.2. Parallel pre-compute correlator with pipelining

3. RESULTS AND DISCUSSIONS

Simulation is done using Xilinx ISE 13.2 tool using Verilog HDL (Verification Logarithmic Hardware Description Language) and it has been synthesized on Kintex7 (xc7k70t-fbg676) FPGAs for the multiplier less correlator and pre-compute correlator.

Simulation Result of Parallel Pre-compute Correlator: The simulation result of parallel precompute correlator is shown in Fig. 3. Here X is 32 bit input. H1,h2,….h64 are correlator coefficients. Y_re and y_img are the real and imaginary part of the correlator outputs. Various inputs are given and associated outputs are analyzed.

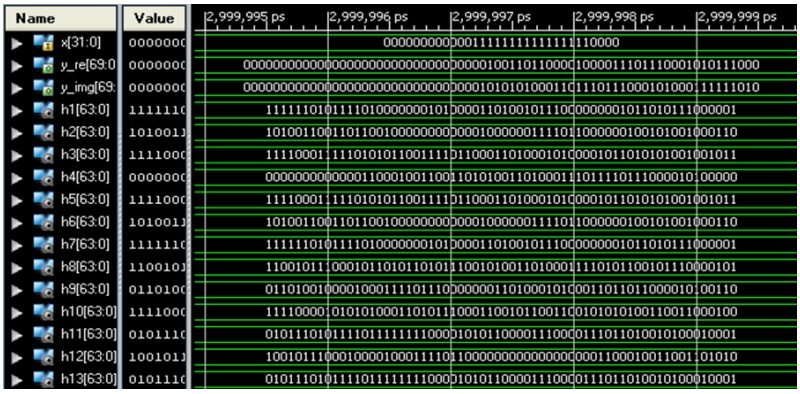

Figure.3. Simulation Result of Parallel Precompute Correlator

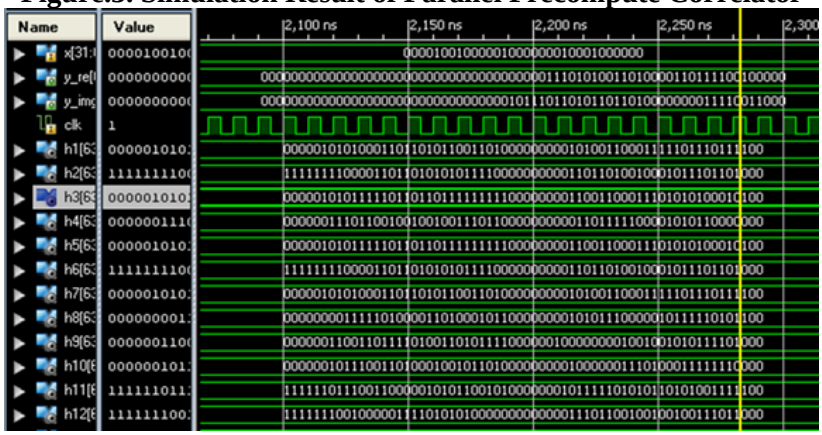

Figure.4. Simulation Result of Parallel Precompute Correlator with Pipelining

Simulation Result of Parallel Precompute Correlator with Pipelining: The simulation result of parallel precompute correlator with pipelining is shown in Fig.4. Here x is the 32 bit input. Clk is the clock input and h1, h2….h64 are complex correlator coefficients. Y_re and y_img are the real and imaginary part of the correlator outputs.

Implementation Results: The architecture of precompute correlator with VLSI optimization techniques auch as parallel processing and pipelining is synthesized on Kintex 7 FPGA using Xilinx ISE 13.2. These architectures are coded using Verilog HDL.

Table.1. Comparison of Area

Technique	Number of Occupied Slices	Number of Slice LUTs
Correlator using Array Multiplier	**3704**	**12015**
Parallel precompute correlator	2303	9074
Parallel precompute correlator with pipelining	2404	9180

The area overhead is analysed in terms of number of occupied slices and number of slice LUTs and given in Table.1. From the obtained results, it is clear that the Parallel precompute correlator reduces the area and inclusion of pipelining slightly increases the area overhead.

Table.2. Comparison of Delay

Technique	Delay (ns)
Correlator using Array Multiplier	28.998
Parallel precompute correlator	19.588
Parallel precompute correlator with pipelining	16.219

From Table.2, it is clear that, when compared to parallel precompute correlator, parallel precompute correlator with pipelining reduces the delay by 20.77%.

Table.3. Comparison of power

Technique	Power (watts)
Correlator using Array Multiplier	5.219
Parallel precompute correlator	2.5
Parallel precompute correlator with pipelining	2.09

The Table.3. shows that parallel precompute correlator with pipelining reduces the power consumption by 0.7%.

4. CONCLUSION

The techniques of pipelining and parallel processing have been discussed. Which technique to employ in a specific design depends on factors such as functionality, chip area, power consumption and complexity of the control logic. Up to certain limit pipelining provides significant performance gains with little increase in chip area. It also reduces glitching in the circuit. Throughput beyond that acheivable by pipelining can be attained by parallel architectures. For parallel architectures the throughput scales almost linearly with chip area. When compared to parallel pre-compute correlator, parallel pre-compute correlator with pipelining reduces the delay by 20.77%.

In future recent optimization techniques like particle swarm optimization, cukoo search algorithm can be adopted for further improving the performance of the correlators.

REFERENCES

Aifeng Ren, Qinye Yin, FPGA Implementation of a W-CDMA System Based on IP Functions, WSEAS Int. Conf. on Dynamical Systems and Control, Venice, Italy, 2005, 320-324.

Alidina M, Monteiro J, Devadas S, Ghosh A, and Papaefthymiou M, Precomputation-based sequential logic optimization for low power, In Proceedings of the 1994 International Workshop on Low Power Design, 2 (4), 1994, 426-436.

Anandh Leno D1, Arul Rex A, Design of Resource Efficient Low Power Correlator for Communication, International Journal of Research in Advent Technology, 2 (2), 2014.

Andrew Fort, Jan- Willem Weijers, Veerle Derudder, Wolfgang Eberle, Andre' Bourdoux, A Performance And Complexity Comparison Of Auto-Correlation And Cross-Correlation For OFDM Burst Synchronization, IEEE International Conference, 2003, 341-344.

Devgan A and Nassif S, Power Variability and its Impact on Design, In International Conference on VLSI Design, 2005, 679–682.

Fatemeh Kashfi, Safar Hatami, Massoud Pedram, Multi-Objective Optimization Techniques for VLSI Circuits, Quality Electronic Design (ISQED), 12th International Symposium, 2011, 1 – 8.

Hazari G and Narayanan H, On the Use of Simple Electrical Circuit Techniques for Performance Modeling and Optimization in VLSI Systems, IEEE Transactions On Very Large Scale Integration (VLSI) SYSTEMS, 19 (10), 2011, 1861-1873.

Jongmin Cho, Jinsang Kim, and Won-Kyung Cho, VLSI Implementation of Auto-Correlation Architecture for Synchronization of MIMO-OFDM WLAN Systems, Journal Of Semiconductor Technology And Science, 10 (3), 2010, 185-192.

Nielsen L.S, Niessen C, Sparso J and van Berke C.H, Low-power operation using self-timed circuits and adaptive scaling of the supply voltage, IEEE Transactions on VLSI Systems, 2 (4), 1994, 391-397.

Sivasankari B and Poongodi P, Design of Low Power and High Speed Correlators for IEEE 802.16 WiMAX Systems, Circuits and Systems, **7**, 2016, 1352-1360.

Thinh H, Pham, Suhaib A, Fahmy, and Ian Vince McLoughlin, Low-Power Correlation for IEEE 802.16 OFDM Synchronization on FPGA, IEEE Transactions On Very Large Scale Integration (VLSI) Systems, 21 (8), 2013, 1549 – 1553.

Trishali, Hiwarkar S, Sunil R, Gupta, Efficient Correlator for OFDM Synchronization on FPGA Implementation, International Journal on Recent and Innovation Trends in Computing and Communication 3 (7), 2015, 4377-4381.

Uttraphan C, Shaikh-Husin N, Khalil Han M, An Optimization Algorithm for Simultaneous Routing and Buffer Insertion with Delay-Power Constraints in VLSI Layout Design, Quality Electronic Design (ISQED), 15th International Symposium, 2014, 357 – 364.

Visweswariah C, Optimization Techniques for High-Performance Digital Circuits, In International Conference on Computer Aided Design, 1997, 198–207.